

# Breaking and Fixing Speculative Load Hardening

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# Outline

**Zhiyuan Zhang**, Gilles Barthe, Chitchanok Chuengsatiansup, Peter Schwabe, Yuval Yarom, “Breaking and Fixing Speculative Load Hardening”, eprint <https://eprint.iacr.org/2022/715>.

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Attack

Mitigation

Semantic Proof

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- Speculative Execution
- Spectre Attack and Speculative Load Hardening (SLH)
- Break SLH via control flow transfer and variant-time executions
- Fix SLH → Ultimate SLH and performance evaluation

# Speculative Execution

```
if (index < arrayLen) {  
    x = array[index];  
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## Resolve condition takes time

- Compute condition
- Fetch value from main memory

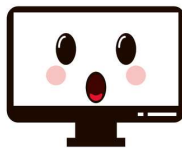


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Let's predict the branch condition

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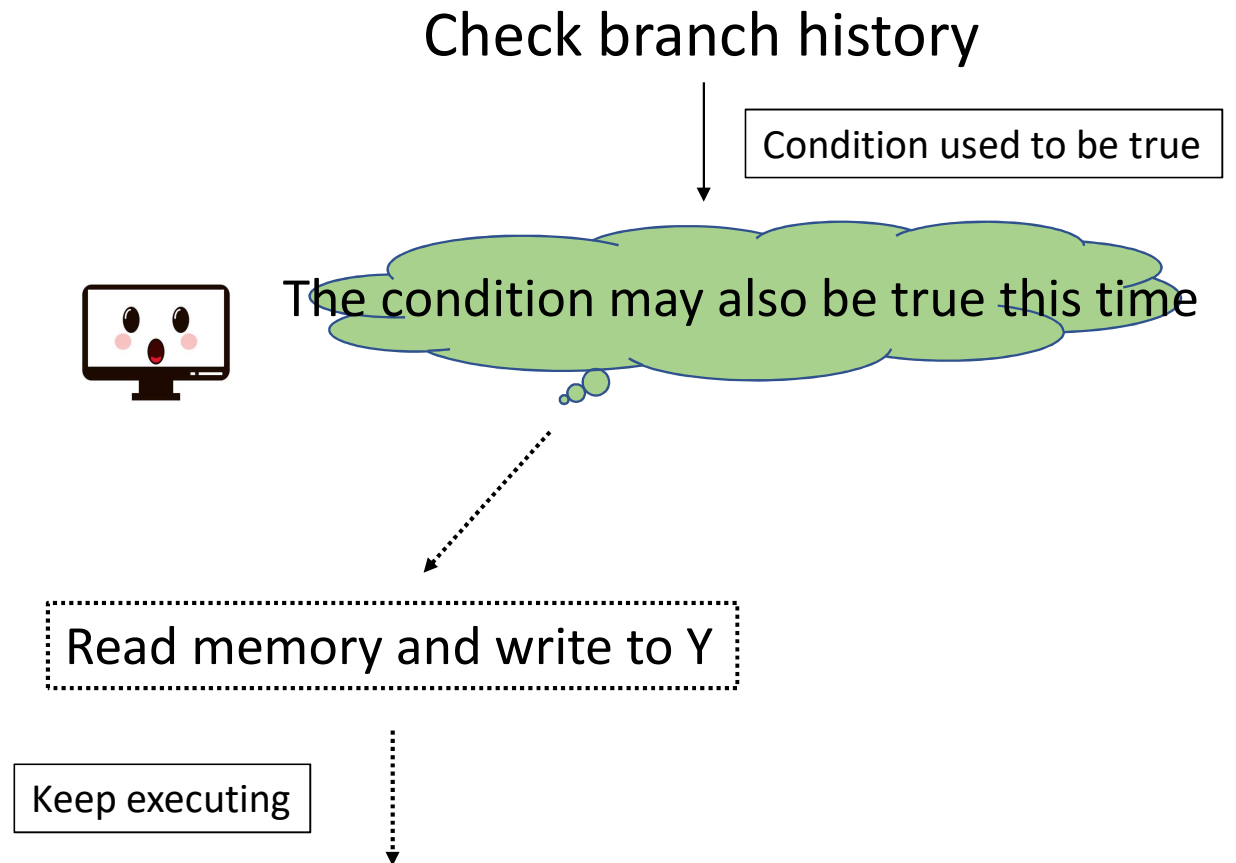
Check branch history

Condition used to be true

The condition may also be true this time

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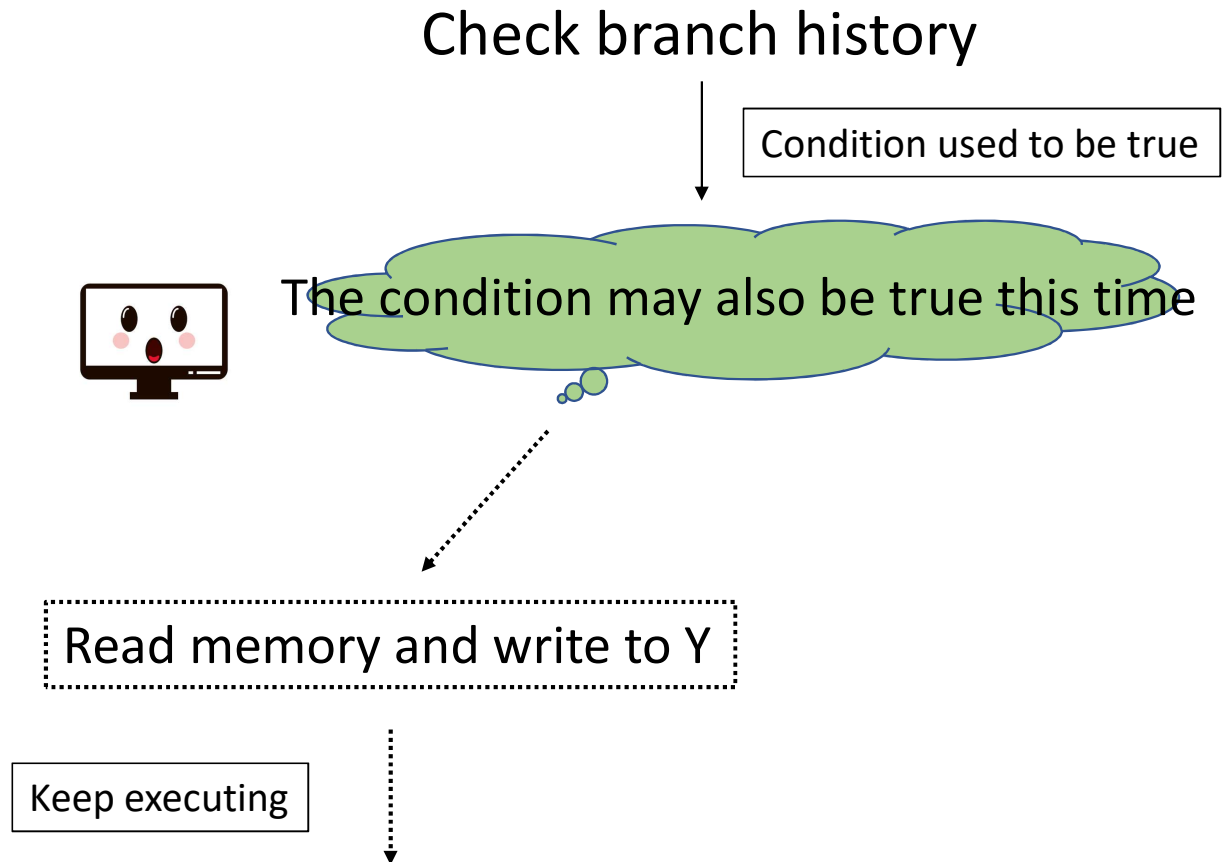
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# Speculative Execution

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if (index < arrayLen) {  
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After a while, the condition is resolved to be true



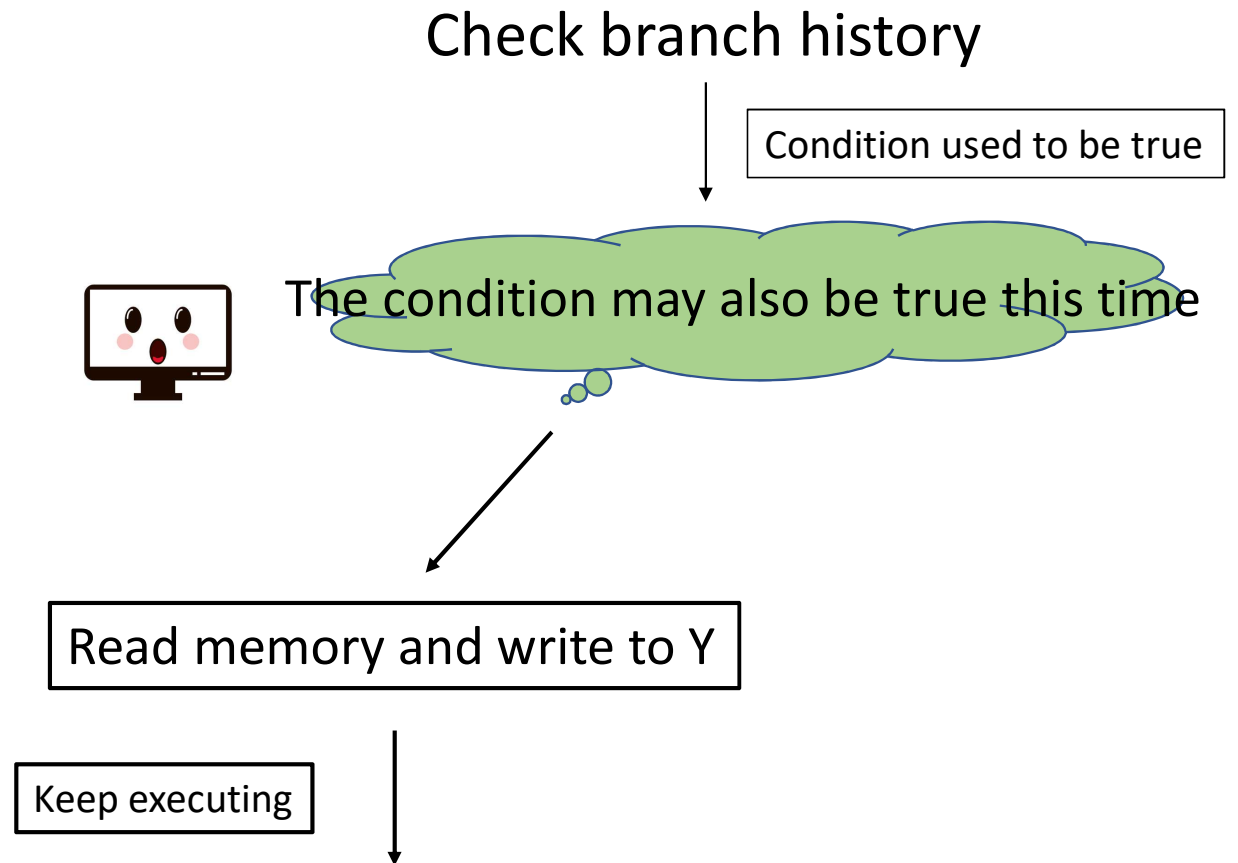
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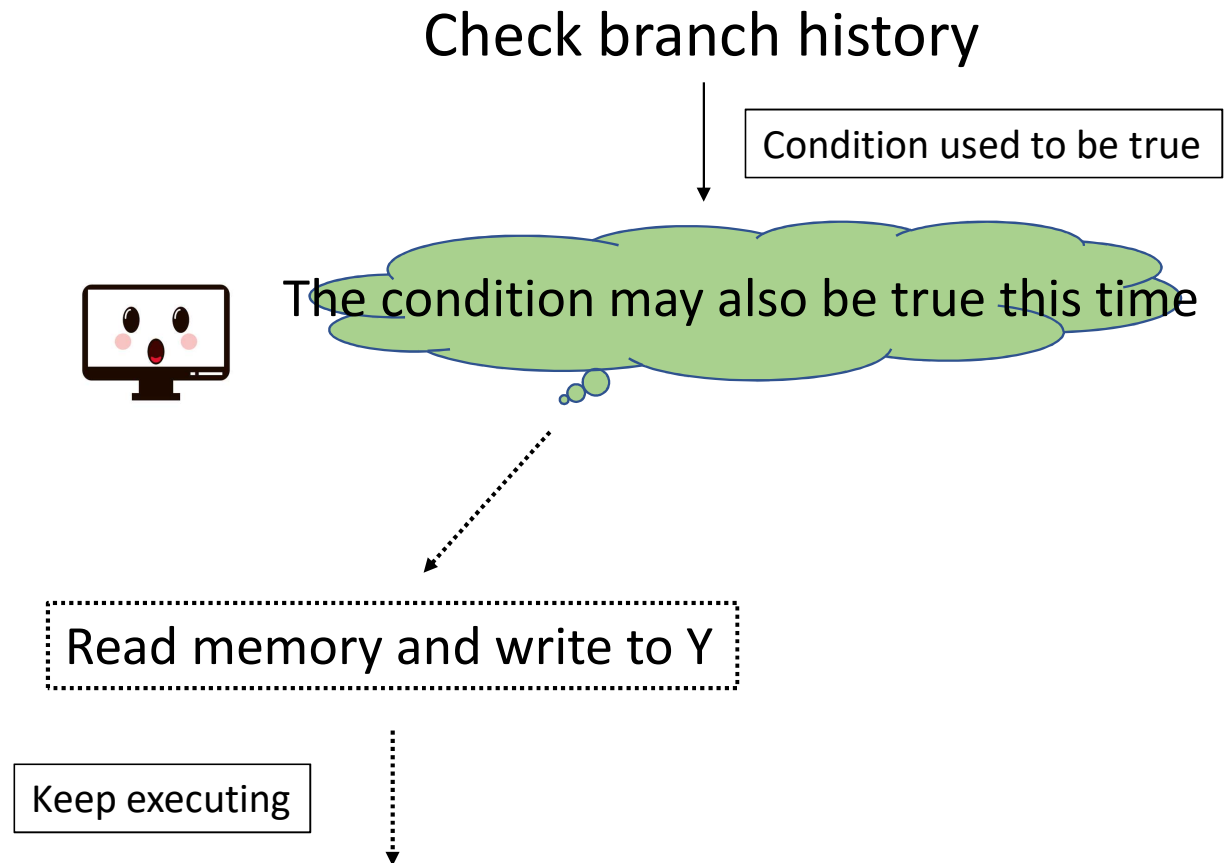
Let's retire these executions



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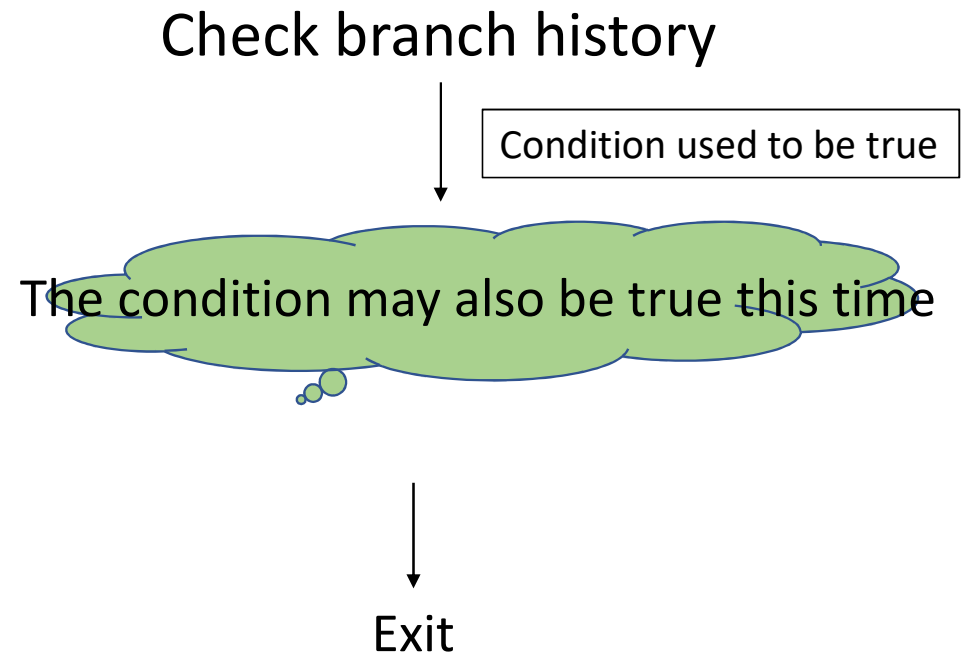
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Let's squash these executions, start executing on the correct path



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Let's squash these executions, start executing on the correct path



The condition may also be true this time

Check branch history

Condition used to be true

Exit



Don't want misprediction next time, update branch history



# Spectre Attack

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I want to leak entire virtual space memory.  
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The speculative execution is based on branch history.  
I think I could poison the branch history...

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Keep feeding in-bound index

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I rollback all executions.



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The cache status has been changed



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You leak architecture changes

- Cache status
- Execution port contention
- Power consumptions
- .....

The cache status has been changed



Keep feeding in-bound index

Flush arrayLen

Flush array2

Feed an out-of-bound index



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# Speculative Load Hardening (SLH)

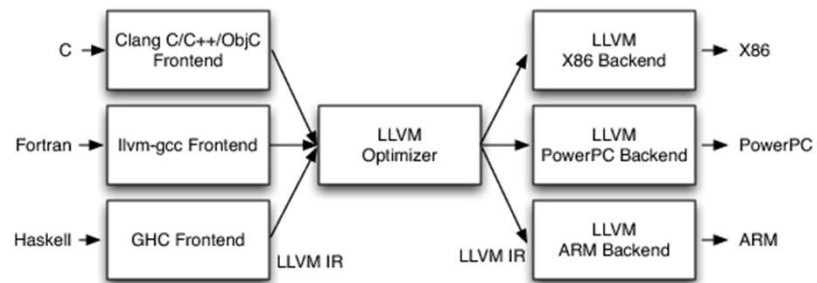
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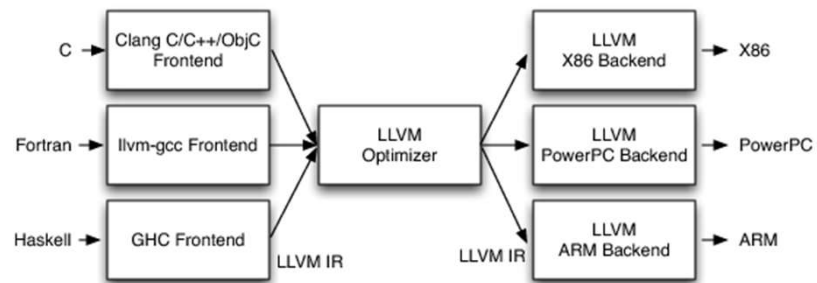
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Track speculative state

Poison loaded value / address

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Track speculative state

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Conditional update cannot be speculated

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if (index < arrayLen) {
    mask = index < arrayLen ? mask : -1;
    x = array[index] | mask;
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Poison the value with -1 to avoid race condition between flushing the pipeline and loading memory

# Limitation of SLH

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- SLH **only** hardens memory reading
- Leaks could from
  - Control flow transfer
  - Speculative store
  - Limited execution resources
    - Execution Ports
    - Reservation Station
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```
victim(int value, int isPublic) {  
    if (isPublic) {  
        //Leaky code  
    }  
}
```

Leak via control flow transfer

# Leak via control flow transfer

```
// Boundary Check
if (isPublic) {
    if (value == 0) {
        a2 = a1 | a2;
        a3 = a2 | a3;
        ...
    } else {
        a1 = crc32(a1, a1);
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```



# Leak via control flow transfer



Flush the outer branch

- Brings > 150 cycles speculation window

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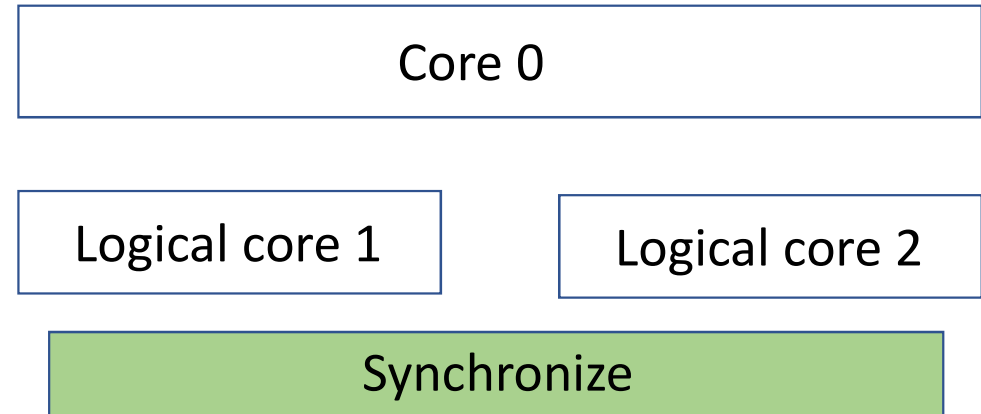
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Instructions are sent to various execution ports  
I measure which port is being used.

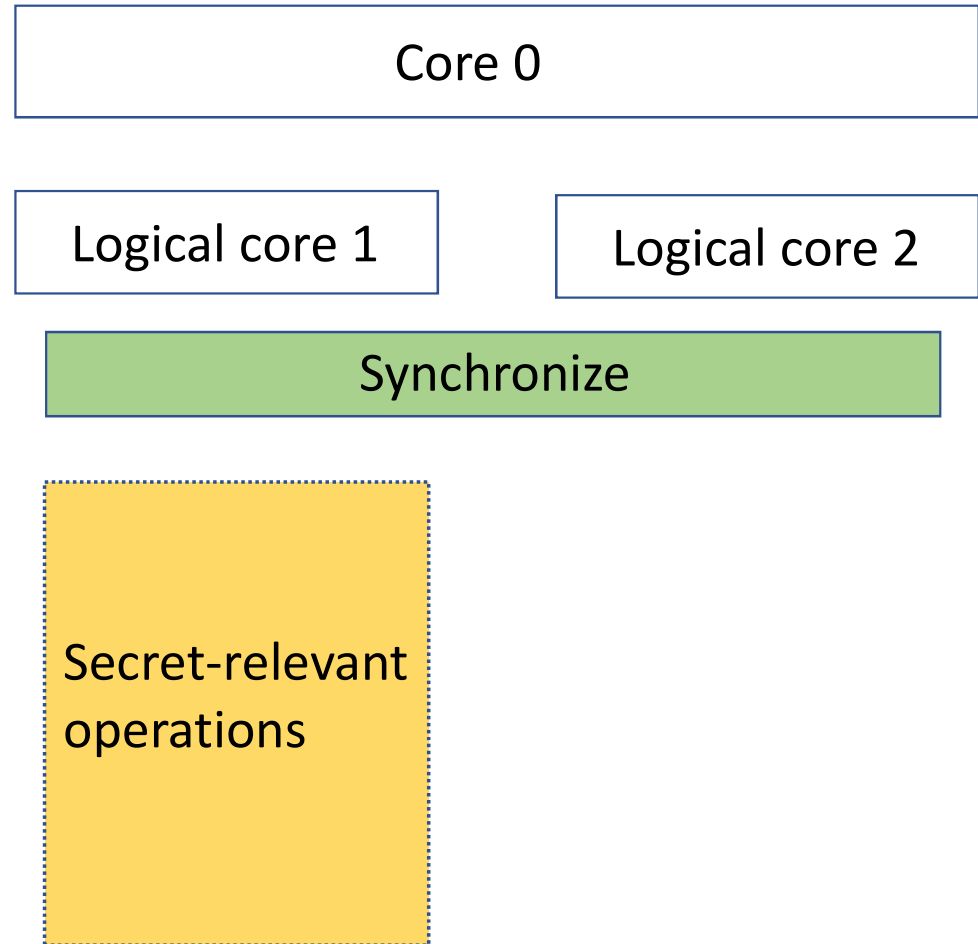
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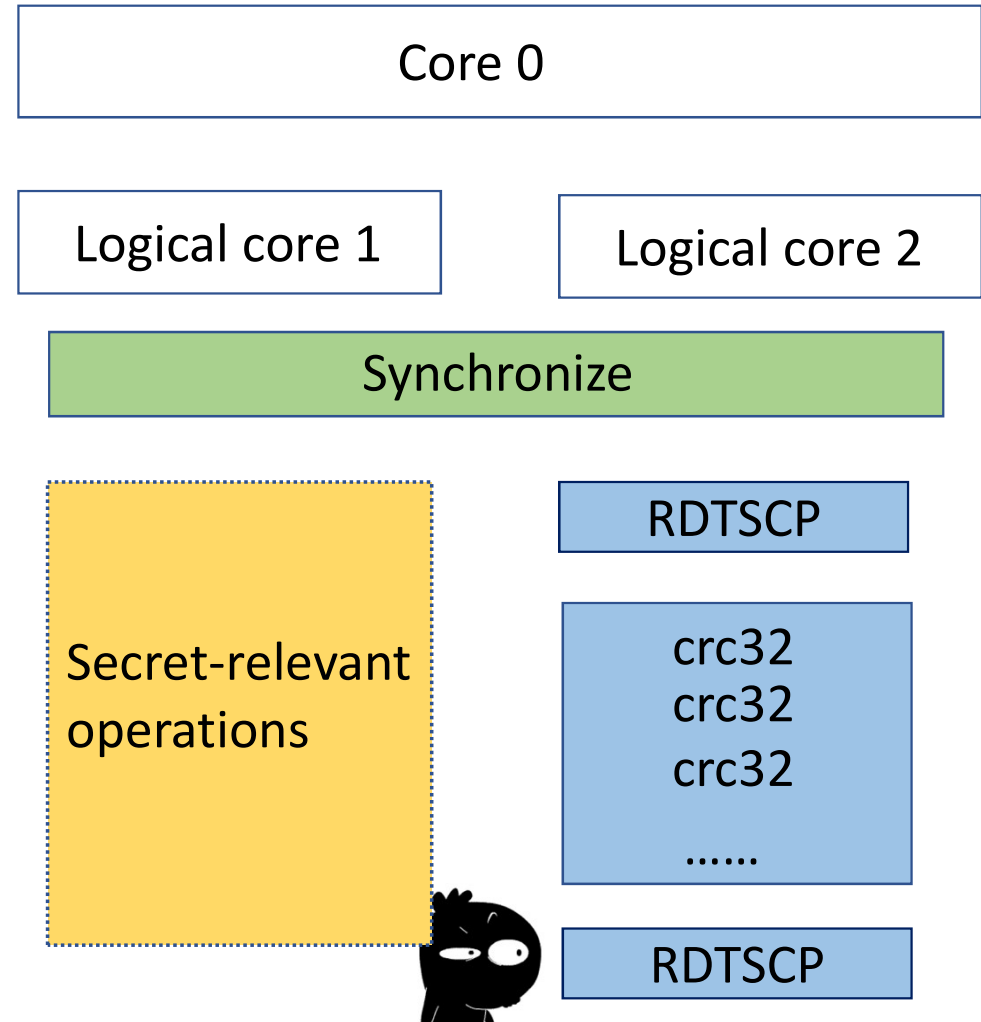
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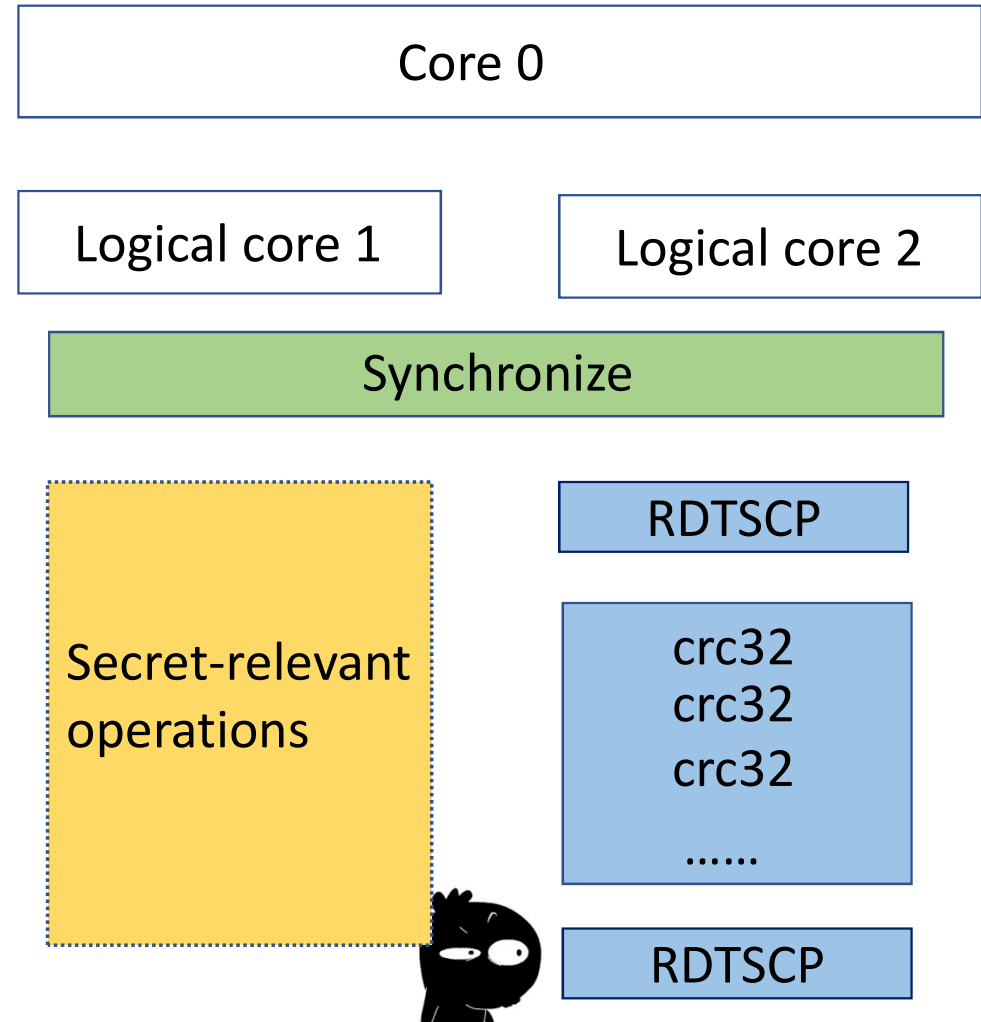
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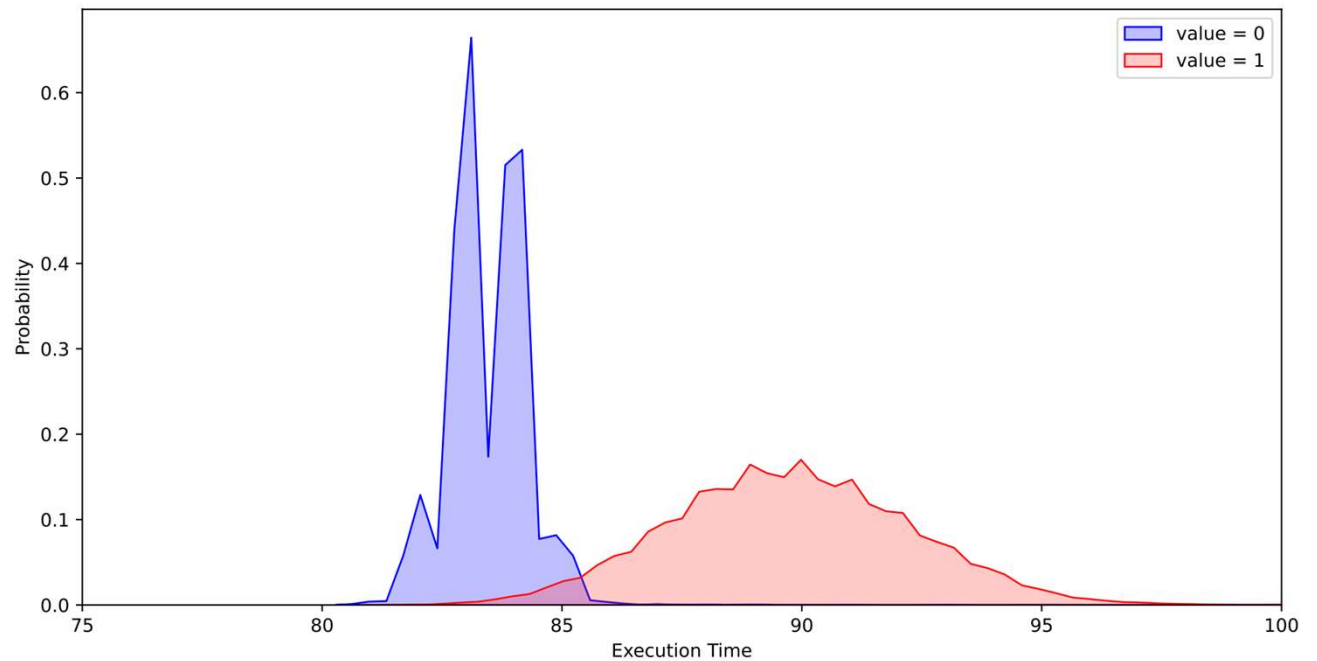
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# Fix SLH

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        ...  
    }  
}
```

# Fix SLH

```
// Boundary Check  
mask = 0;  
if (isPublic) {  
    mask = isPublic ? mask : -1;  
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```

Compiled by SLH



# Fix SLH

```
// Boundary Check
mask = 0;
isPublic |= mask;
if (isPublic) {
    mask = isPublic ? mask : -1;
    value |= mask;
    if (value == 0) {
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    } else {
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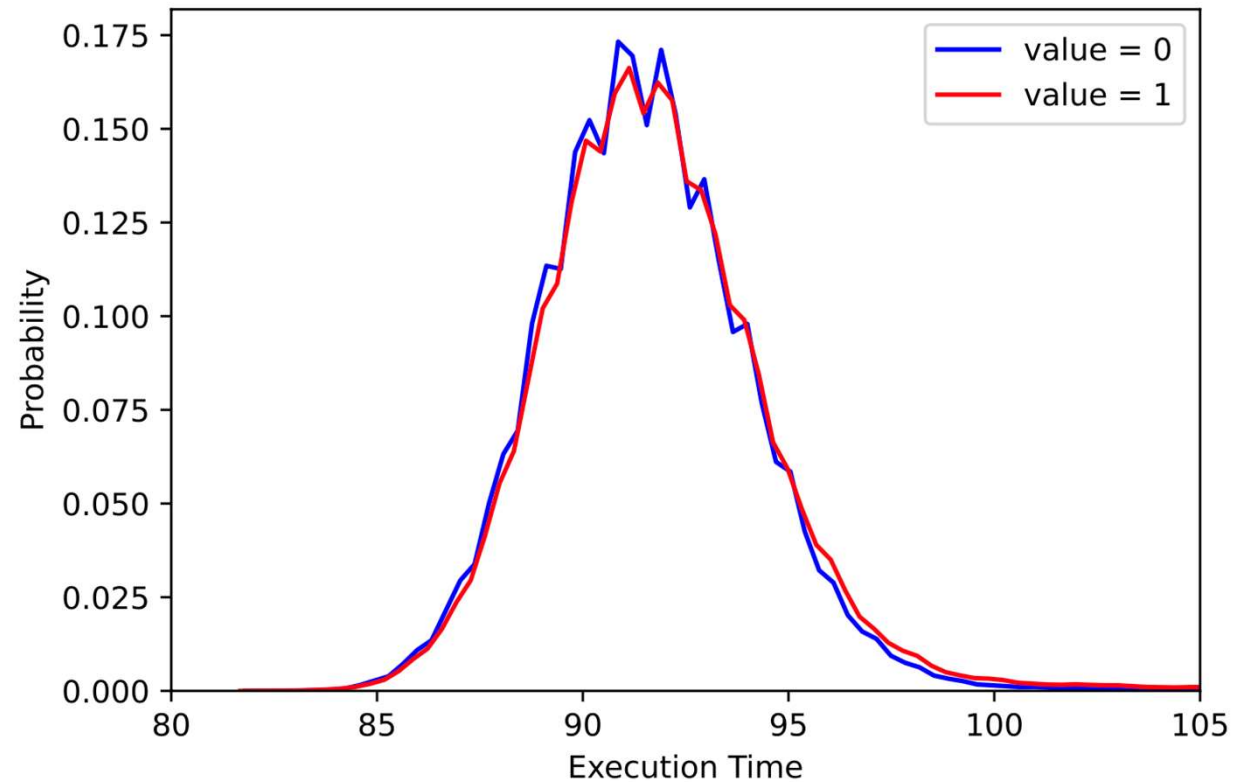
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Compiled by USLH



# Mitigation Result

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On i7-10710U:

Executing a pair of SQRTSD and MULSD:

- 65536: 5 cycles
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Do constant-time  
computing

# Variant-time Instructions



Okay, constant-time computing is slow. I use non-constant-time computing for public data

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The code can be speculatively executed. Measure the execution time.

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I wait until the  
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Constant-time under speculative execution.  
No spectre attacks!

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I doubt it.

# Review pipeline stages

How is an instruction handled by the processor



Front-end

Back-end

# Review pipeline stages

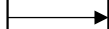
How is an instruction handled by the processor



Front-end

Back-end

Fetch



Decode

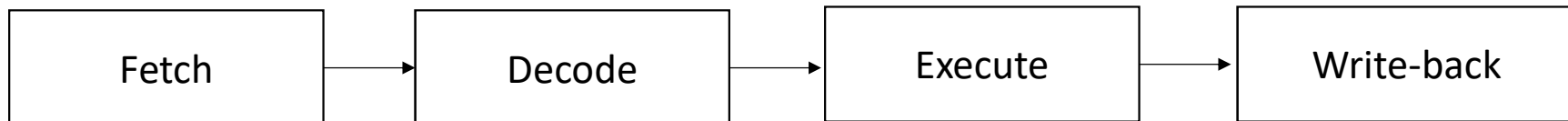
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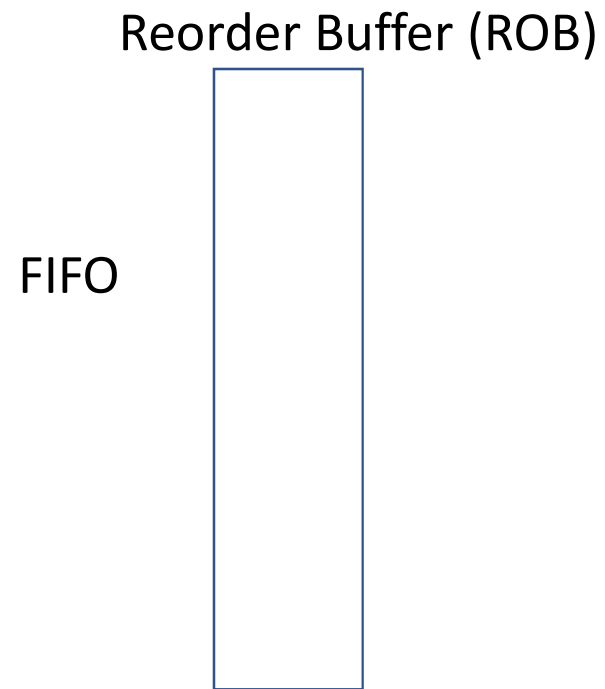


Front-end

Back-end

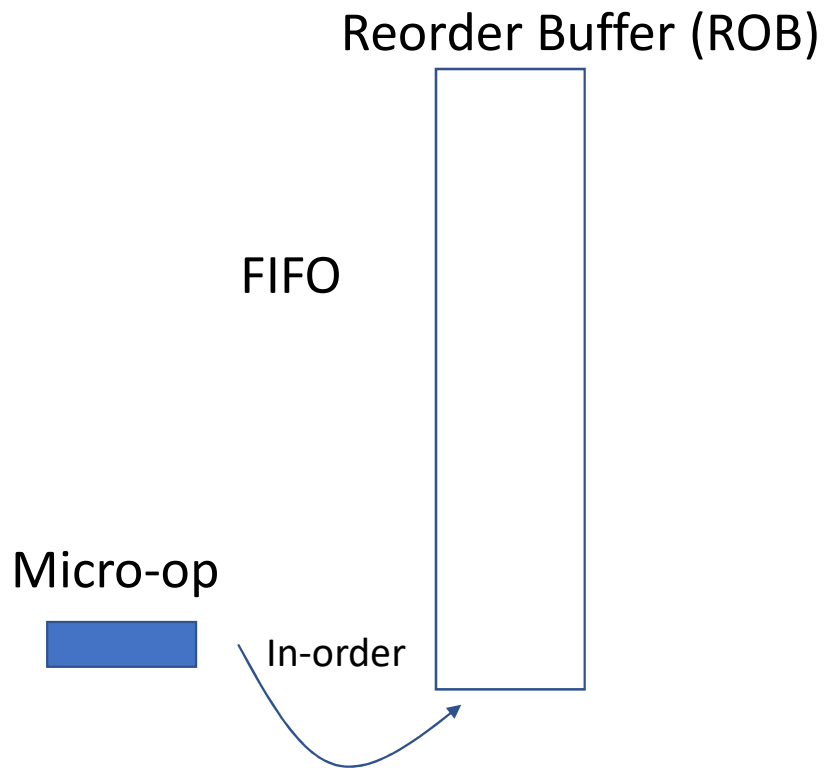


# Execution Engine

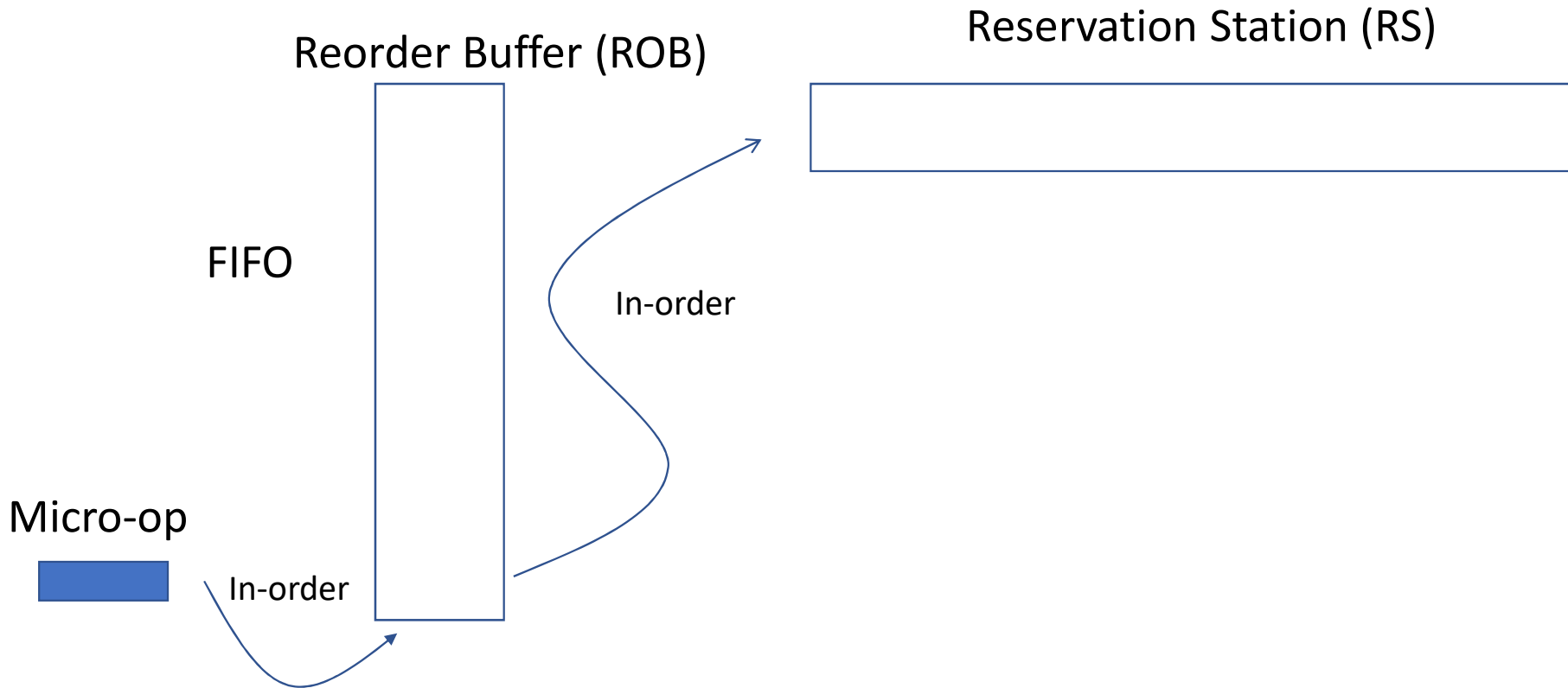




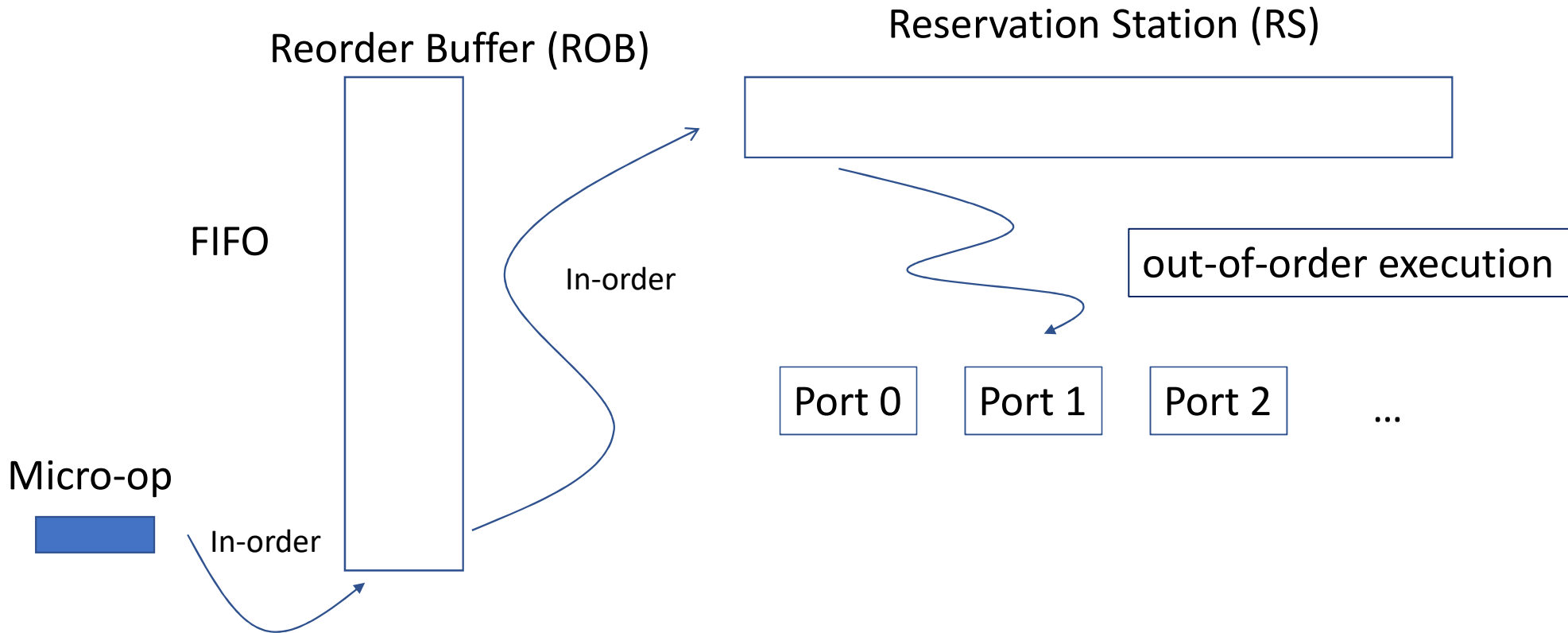
# Execution Engine



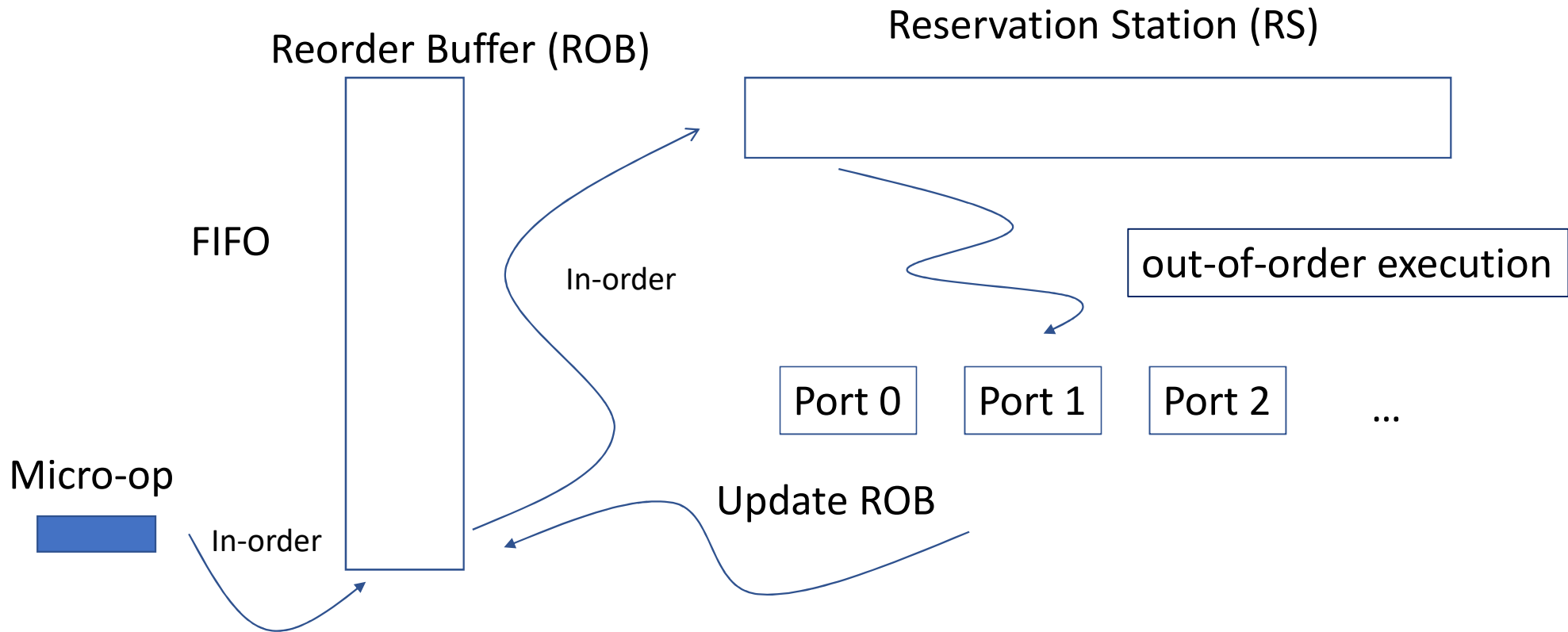
# Execution Engine



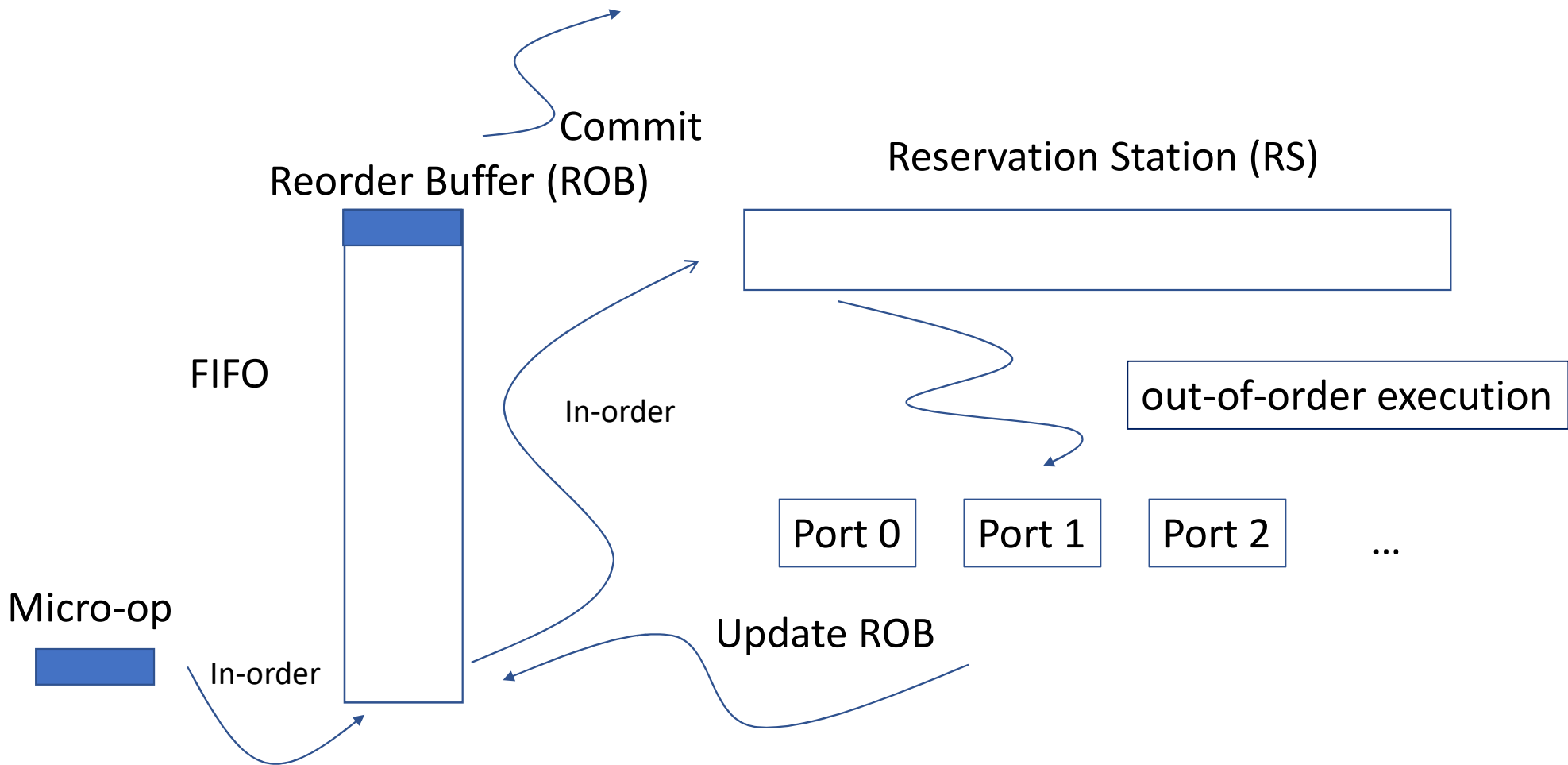
# Execution Engine



# Execution Engine



# Execution Engine



# Execution Engine



ROB and RS has limited Resource

Commit

Reorder Buffer (ROB)

Reservation Station (RS)

FIFO

In-order

out-of-order execution

Port 0

Port 1

Port 2

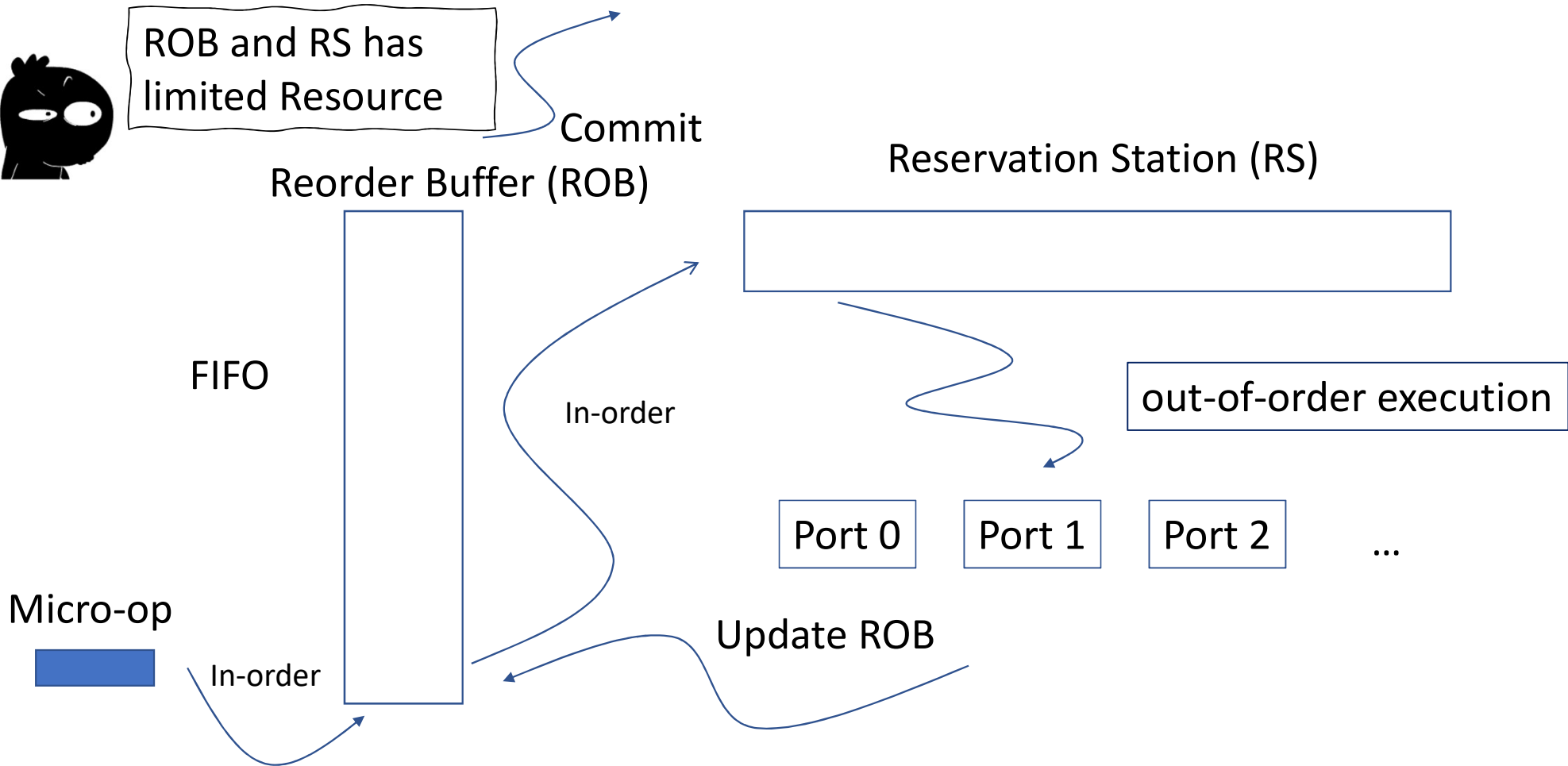
...

Micro-op



In-order

Update ROB



# Variant-time execution under speculation

```
// Boundary Check
```

```
if (isPublic) {  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
}
```

Resolve Branch

ROB

Reservation Station (RS)

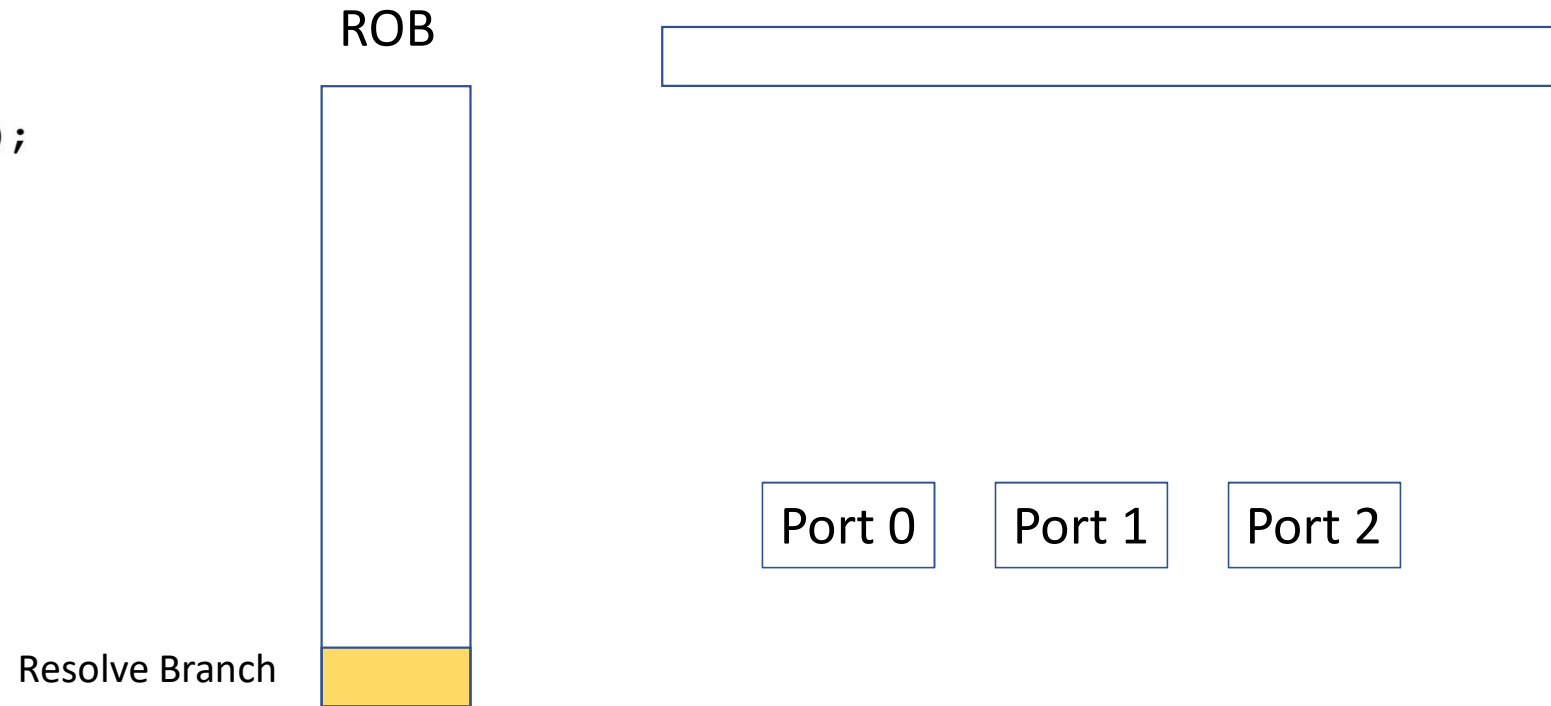
Port 0

Port 1

Port 2

# Variant-time execution under speculation

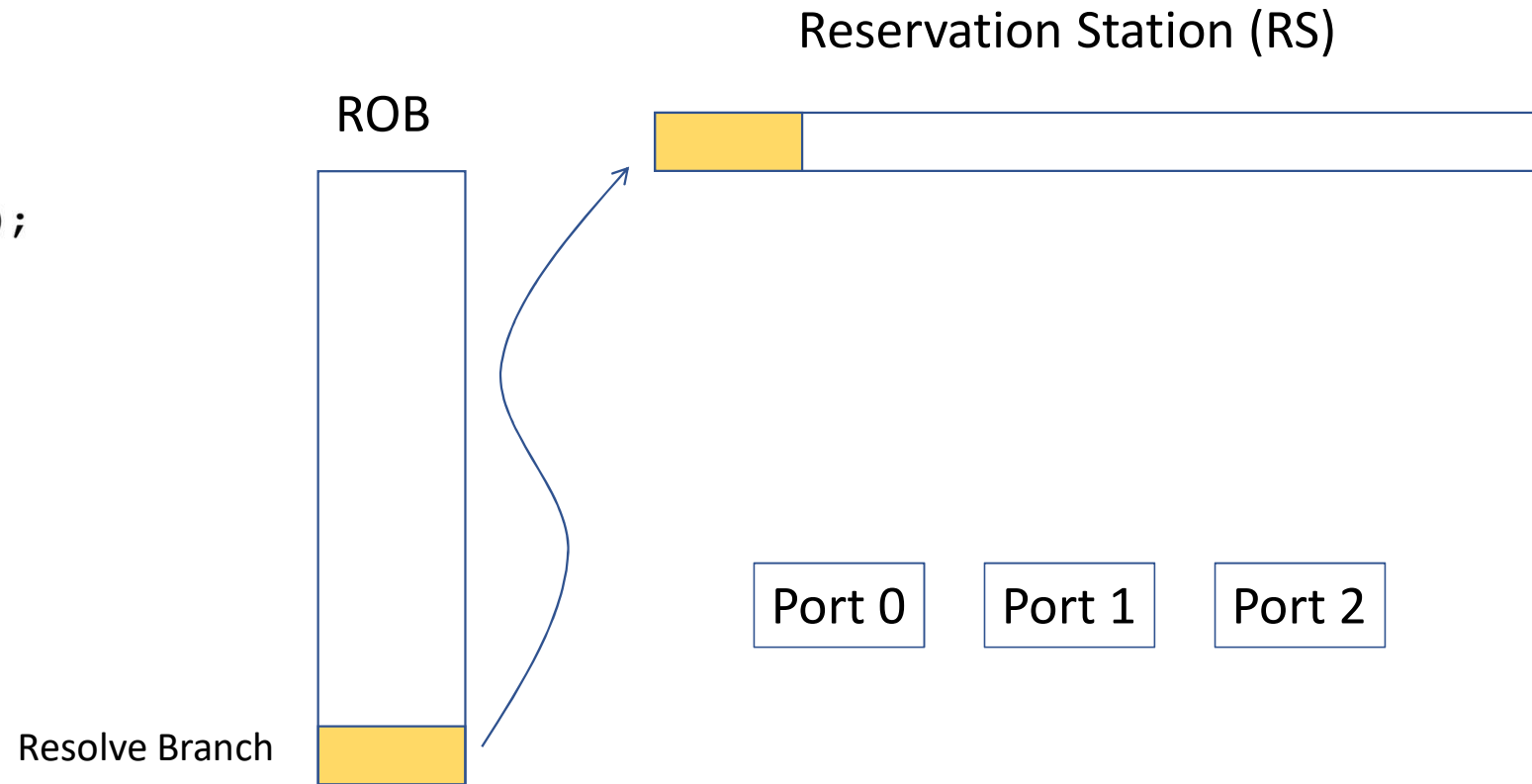
```
// Boundary Check  
if (isPublic) {  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
}
```





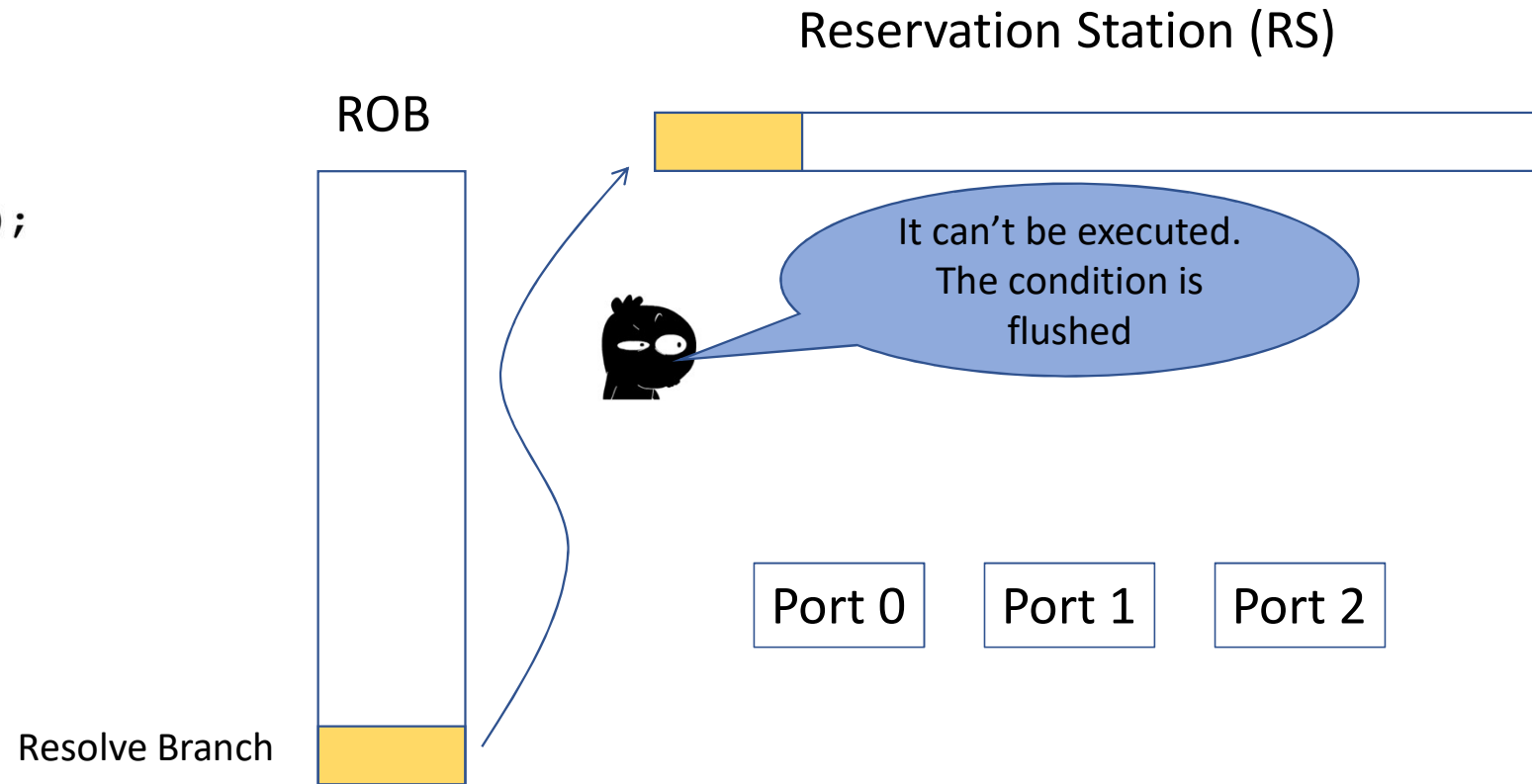
# Variant-time execution under speculation

```
// Boundary Check  
if (isPublic) {  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
}
```



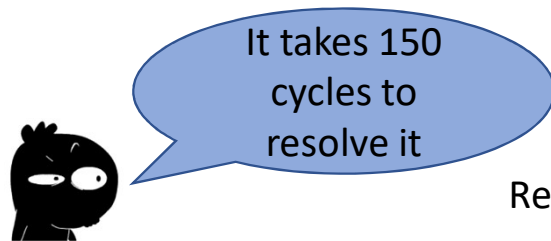
# Variant-time execution under speculation

```
// Boundary Check  
if (isPublic) {  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
}
```



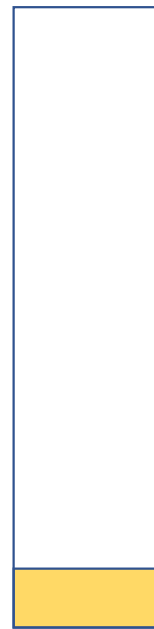
# Variant-time execution under speculation

```
// Boundary Check  
if (isPublic) {  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
}
```



Resolve Branch

ROB



Reservation Station (RS)



It can't be executed.  
The condition is  
flushed

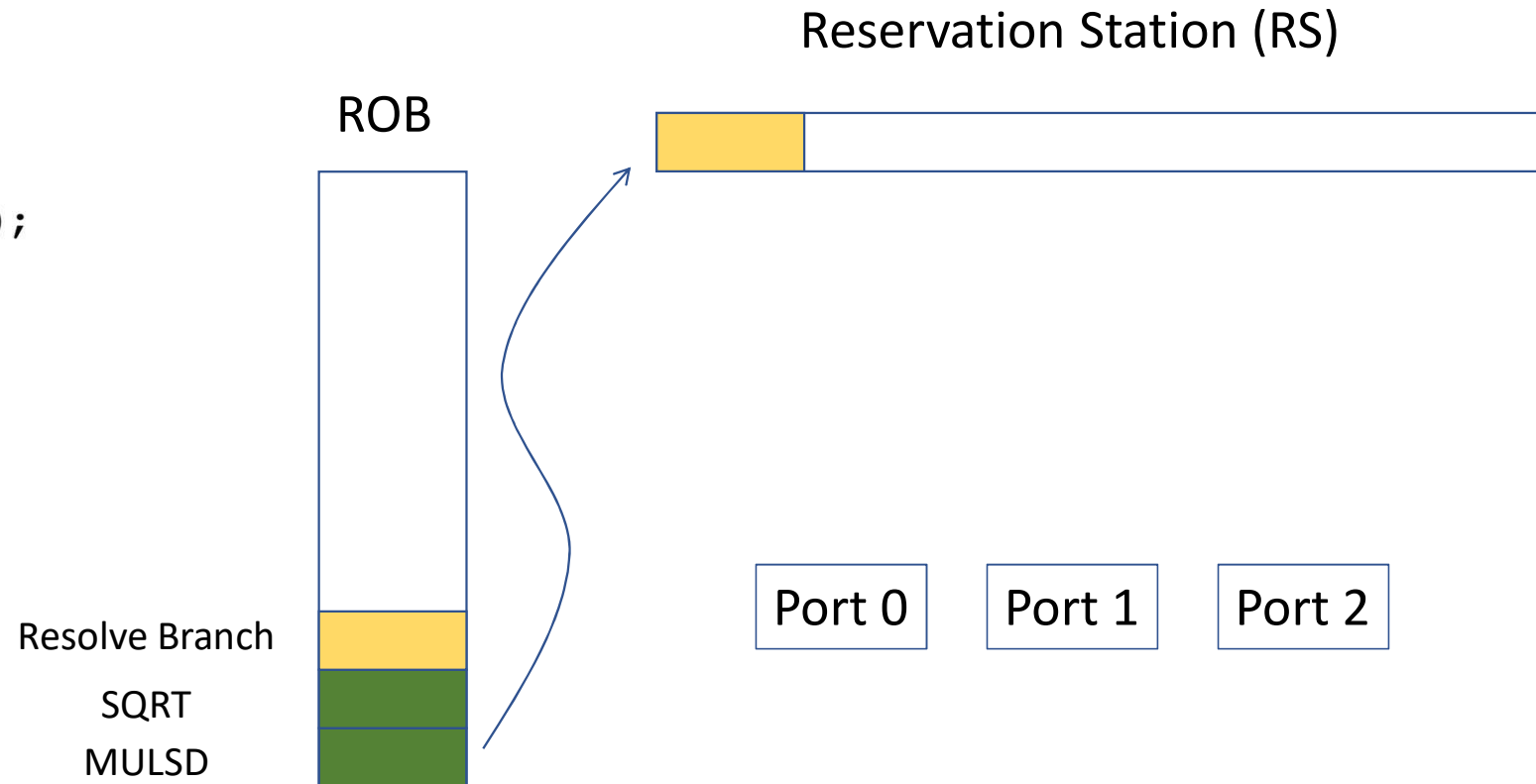
Port 0

Port 1

Port 2

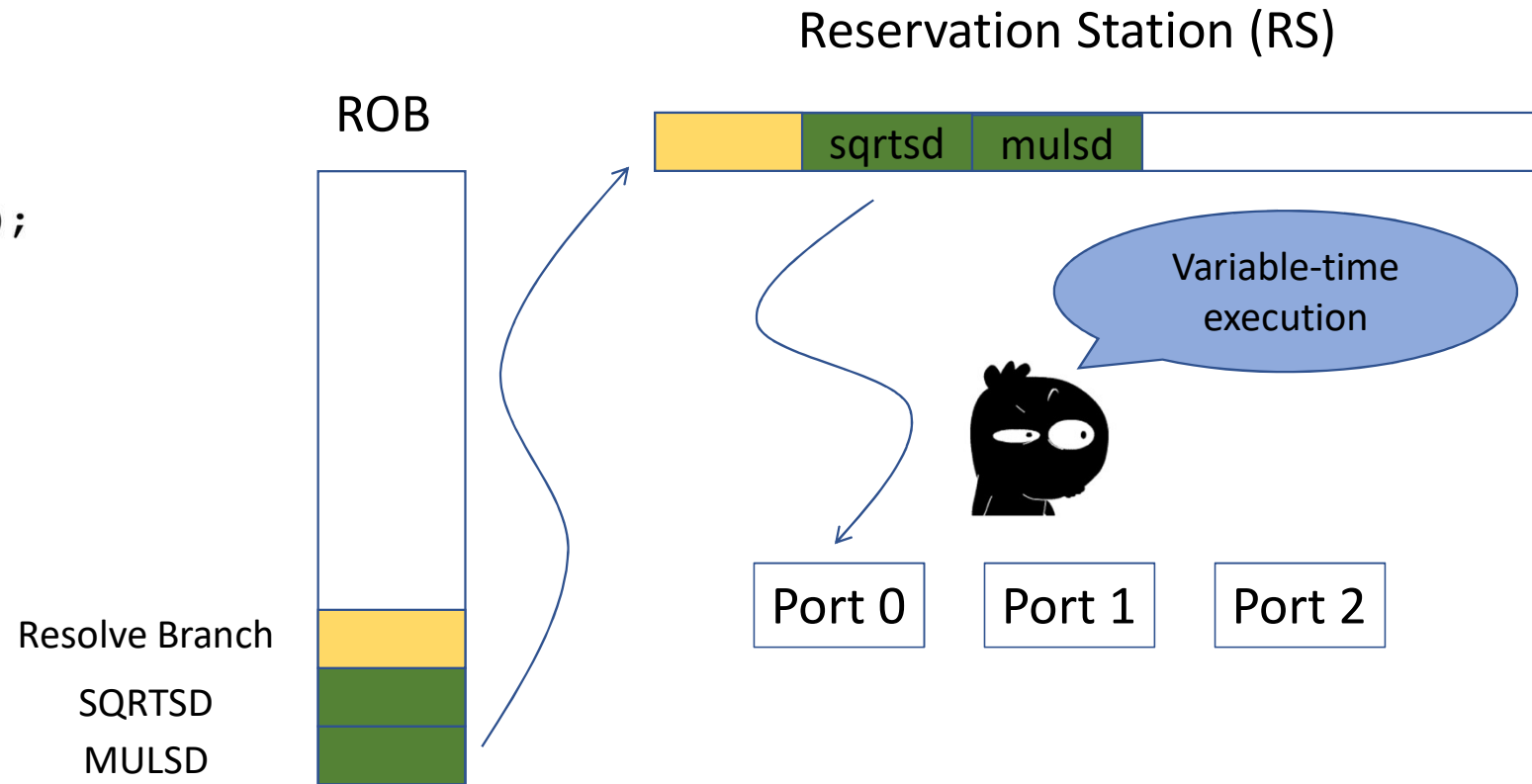
# Variant-time execution under speculation

```
// Boundary Check  
if (isPublic) {  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
}
```



# Variant-time execution under speculation

```
// Boundary Check  
if (isPublic) {  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
}
```



# Variant-time execution under speculation

```
// Boundary Check  
if (isPublic) {  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
}
```



What if we have more variable-time instructions?

Resolve Branch

SQRTSD  
MULSD



Reservation Station (RS)



Port 0



Variable time execution

Port 1

Port 2

# Spectre Attack on variant-time executions

```
// Boundary Check  
if (isPublic) {  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    ...  
}
```

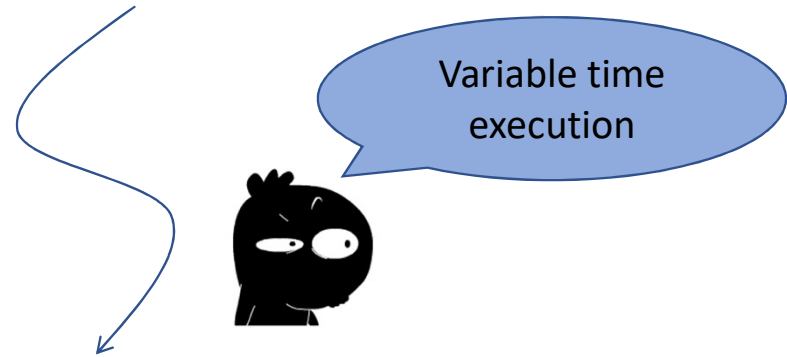


What if we have more variable time instructions?

Resolve Branch  
SQRTSD  
MULSD



Reservation Station (RS)



# Spectre Attack on variant-time executions

```
// Boundary Check
```

```
if (isPublic) {  
  value = sqrtsd(value);  
  value = mulsd(value, value);  
  value = sqrtsd(value);  
  value = mulsd(value, value);  
  ...  
}
```

Resolve Branch  
SQRTSD  
MULSD

Independent  
instructions

ROB



Reservation Station (RS)



Port 0

Port 1

Port 2



# Spectre Attack on variant-time executions

```
// Boundary Check
```

```
if (isPublic) {  
  value = sqrtsd(value);  
  value = mulsd(value, value);  
  value = sqrtsd(value);  
  value = mulsd(value, value);  
  ...  
}
```



Instructions in  
ROB is always  
fixed

Independent  
instructions

ROB



Resolve Branch  
SQRTSD  
MULSD

Reservation Station (RS)



Port 0

Port 1

Port 2

# Spectre Attack on variant-time executions

```
// Boundary Check
```

```
if (isPublic) {  
  value = sqrtsd(value);  
  value = mulsd(value, value);  
  value = sqrtsd(value);  
  value = mulsd(value, value);  
  ...  
}
```



Instructions in  
ROB is always  
fixed

Independent  
instructions

Resolve Branch  
SQRSD  
MULSD

ROB



Reservation Station (RS)



RS will be filled  
up

Port 0

Port 1

Port 2

# Spectre Attack on variant-time executions

```
// Boundary Check
```

```
if (isPublic) {  
  value = sqrtsd(value);  
  value = mulsd(value, value);  
  value = sqrtsd(value);  
  value = mulsd(value, value);  
  ...  
}
```



Instructions in ROB is always fixed



Independent instruction may be blocked

Independent instructions

Resolve Branch  
SQRSD  
MULSD

ROB



Reservation Station (RS)



RS will be filled up



Port 0

Port 1

Port 2

# Spectre Attack on variant-time executions

```
// Boundary Check  
if (isPublic) {  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    ...  
    independent_memory_access(adrs);  
}
```



Instructions in ROB is always fixed



Independent instruction may be blocked

Independent instructions

ROB



Resolve Branch  
SQRSD  
MULSD

Reservation Station (RS)



RS will be filled up

Port 0

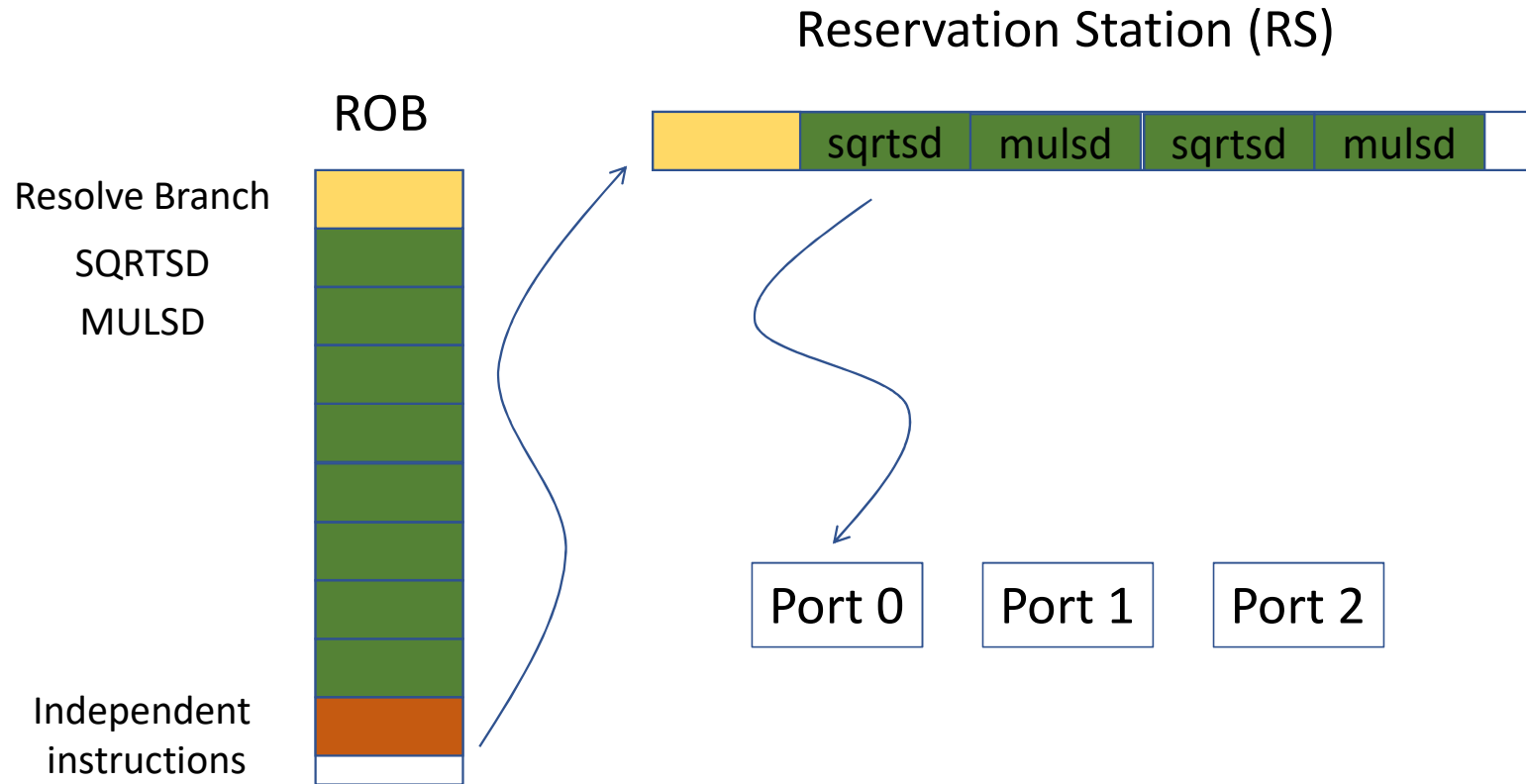
Port 1

Port 2

# Spectre Attack on variant-time executions

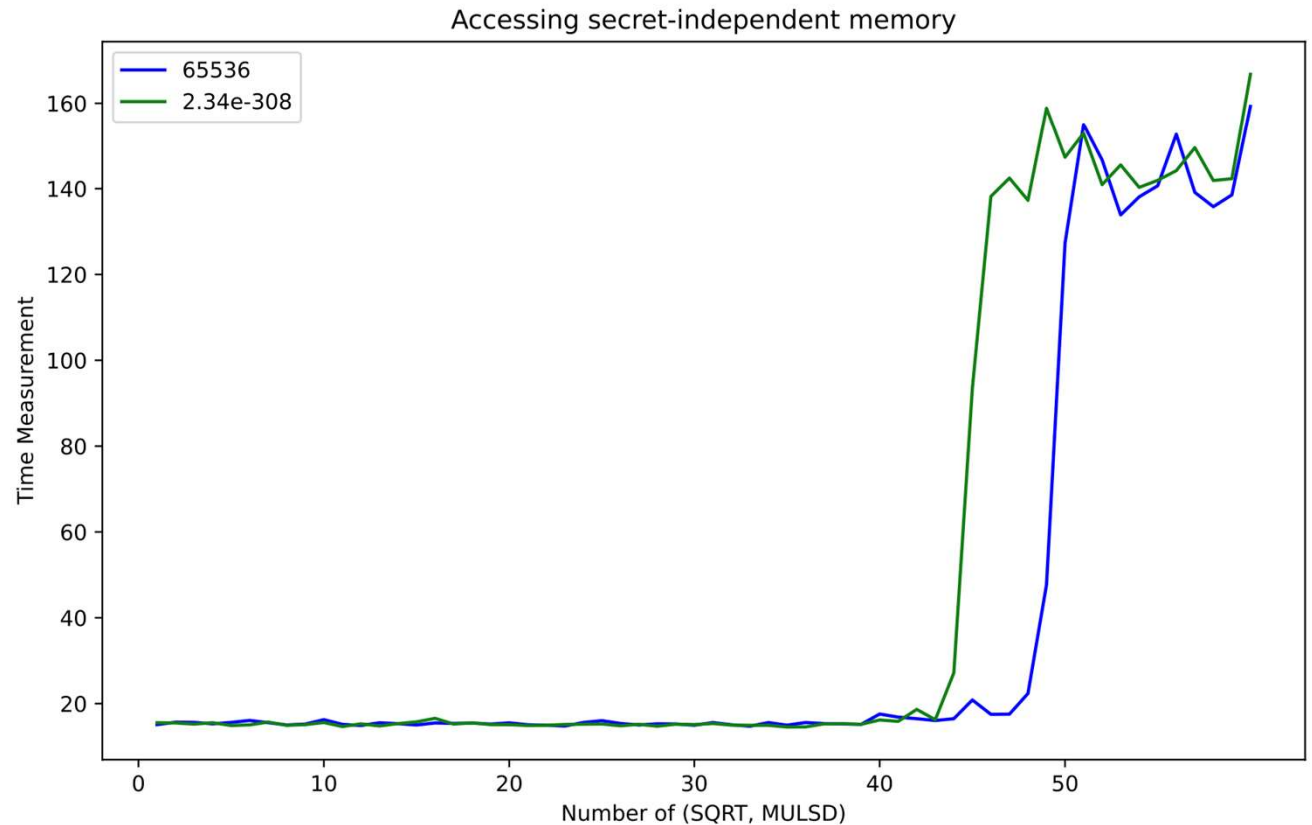
```
// Boundary Check  
if (isPublic) {  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    ...  
    independent_memory_access(adrs);  
}
```

the load may not happen, if RS is not freed before the resolve of branch



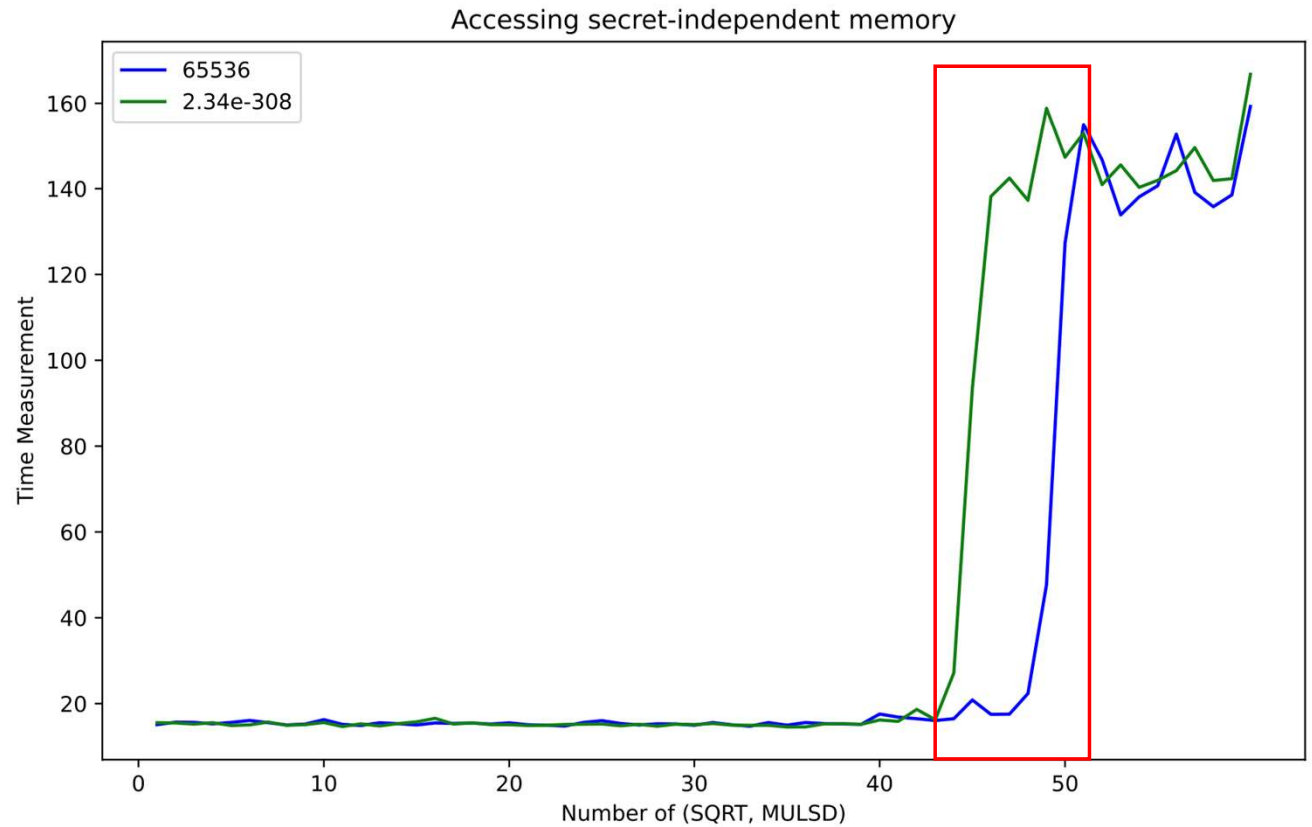
# Limitation of resources

```
victim(double value, int isPublic) {  
    // Branch training  
    for (volatile int i = 0; i < 200; i++);  
  
    // Boundary Check  
    if (isPublic) {  
        value = sqrtsd(value);  
        value = mulsd(value, value);  
        ...  
        value = sqrtsd(value);  
        value = mulsd(value, value);  
        memory_access(adrs);  
    }  
}
```



# Limitation of resources

```
victim(double value, int isPublic) {  
  // Branch training  
  for (volatile int i = 0; i < 200; i++);  
  
  // Boundary Check  
  if (isPublic) {  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    ...  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    memory_access(adrs);  
  }  
}
```



# Fixing SLH

```
// Boundary Check  
if (isPublic) {  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    ...  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    memory_access(adrs);  
}  
}
```



# Fixing SLH

```
mask = 0;  
// Boundary Check  
if (isPublic) {  
    mask = isPublic ? mask : -1;  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    ...  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    memory_access(adrs);  
}
```

Compiled by SLH



# Fixing SLH

```
mask = 0;  
// Boundary Check  
if (isPublic) {  
    mask = isPublic ? mask : -1;  
    value |= mask;  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    ...  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    memory_access(adrs);  
}
```

Compiled by USLH



# Fixing SLH

```
mask = 0;  
// Boundary Check  
if (isPublic) {  
    mask = isPublic ? mask : -1; SQRDSD  
    value |= mask; MULSD  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    ...  
    value = sqrtsd(value);  
    value = mulsd(value, value);  
    memory_access(adrs);  
}
```

Resolve Branch

Independent instructions

ROB



Reservation Station (RS)

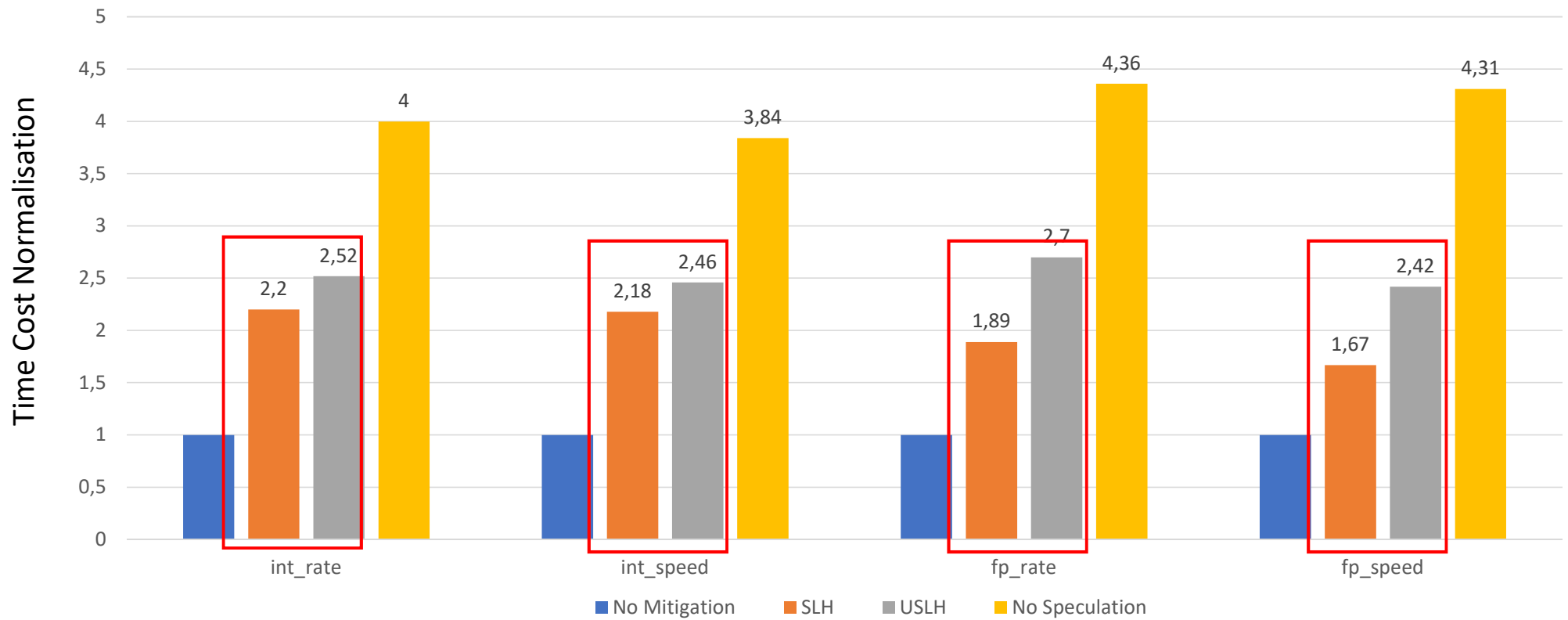


Floating point instructions can only be executed after the resolve of branch condition



# Performance

Benchmark with SPEC2017



# Summary

- SLH is good, but it is not perfect
- Variable-time executions also leak secret in speculative execution
- Accessing a secret-independent memory may also leak information
- USLH costs more, but it is still better than disabling speculative execution